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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,791	12/05/2001	Toshimitsu Tamagawa	103213-00042	2283

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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
Suite 600
1050 Connecticut Avenue, N.W.
Washington, DC 20036-5339

EXAMINER	
JELINEK, BRIAN J	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/001,791	TAMAGAWA, TOSHIMITSU	
	Examiner	Art Unit	
	Brian Jelinek	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

The Examiner respectfully submits a response to the amendment received on 12/8/2005 of application no. 10/001,791 filed on 12/5/2001 in which claims 1, 4-5, and 8 are currently pending.

Arguments

Applicant's amendment and subsequent arguments that Yamashita only shows one dummy photocell per IC chip and does not disclose a plurality of dummy photocells forming an exclusive pair with one of the plurality of image reading photocells, see pg. 9, have been fully considered and are persuasive to overcome the reference as applied. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tsenga.

Applicant's arguments, see pgs. 11-12, with respect to the rejection(s) of claim(s) using Official Notice of outputting a difference between a first and second photoelectric conversion element have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Tseng.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Tseng et al. (U.S. Pat. No. 5,724,094).

Regarding claim 1, Tseng discloses an IC chip for reading an image, comprising: a plurality of image reading photoelectric conversion elements (Fig. 8, sensing elements S1-Sn); a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements (Fig. 9, readout transistors M1); a first signal selection circuit for sequentially selecting the plurality of first transistors (Fig. 8, static shift register); a plurality of dummy photoelectric conversion elements, each of which is arranged in close proximity to and forms and exclusive pair with one of the plurality of image reading photoelectric conversion elements and is shielded from light (Fig. 8, dummy sensors d1-dn); a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements (Fig. 9, readout transistors M1; col. 4, lines 1-21); a second signal selection circuit for sequentially selecting the plurality of second transistors (Fig. 8, static shift register); an output circuit for processing the first and second photoelectric conversion signals and then outputting a resulting signal, wherein the output circuit outputs a difference between the first photoelectric conversion signal from each of the plurality of image reading photoelectric conversion elements, and the second photoelectric conversion signal from the dummy photoelectric conversion element in an

exclusive pair therewith, so as to correct the first photoelectric conversion signal (Fig. 10, differential amplifier).

Regarding claim 4, Tseng discloses an IC chip for reading an image, comprising: a plurality of first processing sections, each comprising: a plurality of image reading photoelectric conversion elements (Fig. 8, sensing elements S1-Sn); a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements (Fig. 9, readout transistors M1); a first signal selection circuit for sequentially selecting the plurality of first transistors (Fig. 8, static shift register); a first signal output line by way of which the first photoelectric conversion signal is transmitted (Fig. 8, video output); a plurality of second processing sections provided so as to pair respectively with the first processing sections, the second processing sections each comprising: a plurality of dummy photoelectric conversion elements, each of which is arranged in close proximity to and forms an exclusive pair with one of the plurality of image reading photoelectric conversion elements and is shielded from light (Fig. 8, dummy sensors d1-dn); a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements (Fig. 9, readout transistors M1; col. 4, lines 1-21); a second signal selection circuit for sequentially selecting the plurality of second transistors (Fig. 8, static shift register); and a second signal output line by way of which the second photoelectric conversion signal is transmitted (Fig. 8, dummy output); an output circuit for processing the first and second photoelectric conversion signals and then outputting a resulting signal; and a signal output line switching circuit for selecting the first and second signal

output lines and connecting the selected first and second signal output lines to the output circuit, wherein the output circuit outputs a difference between the first photoelectric conversion signal from each of the plurality of image reading photoelectric conversion elements, and the second photoelectric conversion signal from the dummy photoelectric conversion element in an exclusive pair therewith, so as to correct the first photoelectric conversion signal (Fig. 10, differential amplifier).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Tseng et al. (U.S. Pat. No. 5,724,094).

Regarding claim 5, Tseng discloses an image reading device comprising: one or more IC chips, each comprising: a plurality of image reading photoelectric conversion elements (Fig. 8, sensing elements S1-Sn); a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements (Fig. 9, readout transistors M1); a first signal selection circuit for sequentially selecting the plurality of first transistors (Fig. 8, static shift register); a plurality of dummy photoelectric conversion elements, each of which is arranged in close proximity to and

forms an exclusive pair with one of the plurality of image reading photoelectric conversion elements and is shielded from light (Fig. 8, dummy sensors d1-dn); a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements (Fig. 9, readout transistors M1; col. 4, lines 1-21); a second signal selection circuit for sequentially selecting the plurality of second transistors (Fig. 8, static shift register); an output circuit for outputting a difference between the first photoelectric conversion signal from each of the plurality of image reading photoelectric conversion elements, and the second photoelectric conversion signal from the dummy photoelectric conversion element in an exclusive pair therewith, as a corrected first photoelectric conversion signal (Fig. 10, differential amplifier); a trigger signal input terminal by way of which a signal for sequentially scanning an image being read is fed in from an IC chip in a previous stage (Fig. 10, SP); a trigger signal output terminal by way of which a signal for sequentially scanning the image being read is fed out to an IC chip in a following stage (Fig. 10, EP); a clock input terminal by way of which a clock is fed in (Fig. 10, clock); and a reference voltage input terminal by way of which a reference voltage for the output circuit is fed in (Fig. 10, VDD) , wherein said one or more IC chips each start scanning the image being read on receiving an input signal at the trigger input terminal thereof, and, on completion of the scanning, outputs, at the trigger output terminal thereof, a signal for continuing sequential scanning to the IC chip in the following stage.

Tseng does not disclose an A/D converter for converting a signal output from the output circuit into a digital signal. However, Official Notice is given that it is old and well

known in the art to convert the output of an image sensor from analog to digital data in order to perform subsequent image processing operations. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have provided the image sensor of Tseng with an A/D converter for converting a signal output from the output circuit into a digital signal in order to perform subsequent image processing operations.

Regarding claim 8, Tseng discloses an image reading device comprising: one or more IC chips, each comprising: a plurality of first processing sections, each comprising: a plurality of image reading photoelectric conversion elements (Fig. 8, sensing elements S1-Sn); a plurality of first transistors for reading a first photoelectric conversion signal from the image reading photoelectric conversion elements (Fig. 9, readout transistors M1); a first signal selection circuit for sequentially selecting the plurality of first transistors (Fig. 8, static shift register); and a first signal output line by way of which the first photoelectric conversion signal is transmitted (Fig. 8, video output); a plurality of second processing sections provided so as to pair respectively with the first processing sections, the second processing sections each comprising: a plurality of dummy photoelectric conversion elements, each of which is arranged in close proximity to and forms an exclusive pair with one of the plurality of image reading photoelectric conversion elements, and is shielded from light (Fig. 8, dummy sensors d1-dn); a plurality of second transistors for reading a second photoelectric conversion signal from the dummy photoelectric conversion elements (Fig. 9, readout transistors M1; col. 4, lines 1-21); a second signal selection circuit for sequentially selecting the

plurality of second transistors (Fig. 8, static shift register); and a second signal output line by way of which the second photoelectric conversion signal is transmitted (Fig. 8, dummy output); an output circuit for outputting a difference between the first photoelectric conversion signal from each of the plurality of image reading photoelectric conversion elements, and the second photoelectric conversion signal from the dummy photoelectric conversion element in an exclusive pair therewith, as a corrected first photoelectric conversion signal (Fig. 10, differential amplifier); a signal output line switching circuit for selecting the first and second signal output lines and connecting the selected first and second signal output lines to the output circuit (Fig. 8, static shift register); a trigger signal input terminal by way of which a signal for sequentially scanning an image being read is fed in from an IC chip in a previous stage (Fig. 10, SP); a trigger signal output terminal by way of which a signal for sequentially scanning the image being read is fed out to an IC chip in a following stage (Fig. 10, EP); and a clock input terminal by way of which a clock is fed in (Fig. 10, clock), wherein said one or more IC chips each start scanning the image being read on receiving an input signal at the trigger input terminal thereof, and, on completion of the scanning, outputs, at the trigger output terminal thereof, a signal for continuing sequential scanning to the IC chip in the following stage.

Tseng does not disclose an A/D converter for converting a signal output from the output circuit into a digital signal. However, Official Notice is given that it is old and well known in the art to convert the output of an image sensor from analog to digital data in order to perform subsequent image processing operations. As a result, it would have

been obvious to one of ordinary skill in the art at the time of the invention to have provided the image sensor of Tseng with an A/D converter for converting a signal output from the output circuit into a digital signal in order to perform subsequent image processing operations.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Jelinek whose telephone number is (571) 272-7366. The examiner can normally be reached on M-F 9:00 am - 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-

Yen Vu can be reached at (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brian Jelinek
2/14/2006

NGOC-YEN VU
PRIMARY EXAMINER